WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory array comprising a plurality of memory cells;

a page buffer section for temporarily storing data to be written into the memory array; and

a masking section for masking at least a portion of data read from the page buffer section.

2. A semiconductor memory device according to claim 1, wherein the masking section masks the portion of the data based on a data bus width in the semiconductor memory device.

3. A semiconductor memory device according to claim 1, wherein:

the masking section comprises a comparison section for comparing a value of an address of the memory array with a value of at least one of a beginning address and an end address of the memory array, when the data is read from the page buffer section; and

whether or not the data is masked is determined based on a result of the comparison by the comparison section.

4. A semiconductor memory device according to claim 1, wherein:

the masking section comprises a matching detection section for determining whether or not an address of the memory array is equal to at least one of a beginning address and an end address of the memory array, when the data is read from the page buffer section; and

whether or not the data is masked is determined based on a result of the determination by the matching detection section.

5. A semiconductor memory device according to claim 1, wherein:

the masking section comprises a counter section for counting the number of pieces of data to be written into the memory array; and

whether or not the data is masked is determined based on a result of the counting by the counter section.

6. A semiconductor memory device according to claim 1, wherein the masking section comprises a deactivation section for deactivating a portion of the data read from the page buffer section.

7. A semiconductor memory device according to claim 1, wherein:

each of the plurality of memory cells is a multi-value memory cell capable of storing at least three values; and

the semiconductor memory device comprises a page mode read section for simultaneously reading some of the plurality of memory cells.